REMARKS

The final Office Action mailed February 10, 2005, and the Advisory Action mailed May 4, 2005, have been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

Subject Matter Indicated Allowed or Allowable

Applicants gratefully acknowledge the indication of allowability of Claim 38, subject to its re-writing in independent form. For the reasons outlined below, it is believed that base claim 36 is allowable on its merits, and re-writing Claim 38 to include the limitations of Claim 38 is therefore unnecessary.

Claim Changes

Changes of a non-substantive nature have been made to Claim 36 so that terms used therein are more consistent with one another.

Rejection(s) Under 35 U.S.C. § 103(a)

Claims 36 – 37 and 39 – 40 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Diorio et al. (U.S. pat. no. 5,990,512) in view of Alavi et al. (U.S. pat. no. 5,844,300).

The Advisory Action characterizes the Applicants' position as one pertaining to non-analogous art. Such a characterization is inaccurate because a non-analogous art argument is one which contends that the art applied in a rejection and the art to which the invention is directed are

non-analogous. In fact, Applicants' position is that the two references—Diordio et al. and Alvali et al.—are *incompatible with each other*, and therefore cannot be properly combined in an obviousness rejection under 35 U.SC. § 103(a).

In the Advisory Action, it was explained that the motivation for combining Diorio et al. and Alavi et al. was given in the Office Action of February 10, 2005, which contended that it would have been obvious to include p+ doped third and fourth regions of Alavi et al. in the second n-well of Diorio et al. because these two patents "are from the same field of endeavor (pFET transistors)," and "the purpose disclosed in Alavi et al. would have been recognized in the pertinent art of Diorio et al." Therefore, it was alleged, "it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the pFET synapse transistor structure as taught by Diorio et al. with the structure having third and fourth p+ doped regions disposed in a second well as taught by Alavi et al. to develop a structure capable of monitoring electrostatic charge." The Advisory Action then elaborates that "Alavi et al. discloses that it is obvious to one of ordinary skill to have a field effect transistor with wells having more than one impurity region with the wells in Figure 5."

However, as explained above, this reasoning in the Office Action and the Advisory Action fails to take into the account the aforementioned incompatibility issues of the two references as previously explained.

As Applicants have noted, Diorio et al. is directed to a device for storing charge as part of its operation, as most clearly seen from the title ("...Mechanism for Long Term Learning"). In contrast, Alavi et al. is directed to a device for monitoring charge buildup during fabrication.

Thus, while both Diorio et al. and Alavi et al. contain pFETs, it cannot be reasonably maintained that such incidental overlap is sufficient to provide motivation to combine their teachings. The Examiner's own reasoning, that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the pFET synapse transistor structure as taught by Diorio et al. with the structure having third and fourth p+ doped regions disposed in a second well as taught by Alavi et al. *to develop a structure capable of monitoring electrostatic charge*" bears this out simply because Diorio et al. is NOT concerned with monitoring electrostatic charge, and therefore the ordinarily skilled artisan working in the different field of memory and learning of Diorio et al. would not look for guidance to the teachings Alavi et al., which is in the field of monitoring electrostatic charge.

Further, the mere disclosure in Alavi et al. of third and fourth p+ doped regions disposed in a second n-well in one device is no guarantee that such features can also be provided and be operable in the second, different device of Diorio et al. Numerous other factors must be taken into account, rendering such a modification far from obvious. For instance, higher differential voltages may be imposed, erecting higher tunneling and injection barriers, and removing the device from a useful operating range. This is particularly apparent because the structure of the Alavi et al. device is at its core an EEPROM, and includes a central transistor 48 having no counterpart in Diorio et al.

Conclusion

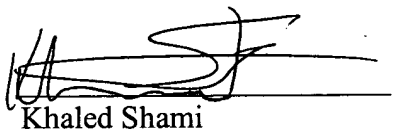
In view of the preceding discussion, Applicants respectfully urge that the claims of the present application define patentable subject matter and should be passed to allowance. Such allowance is respectfully solicited.

If the Examiner believes that a telephone call would help advance prosecution of the present invention, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Reply, or credit any overpayment not otherwise paid or credited, to our deposit account No. 50-1698.

Respectfully submitted,
THELEN REID & PRIEST, L.L.P.

Dated: June 14, 2005



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